WHAT IS CLAIMED IS:

1. A system for performing feedback processing of a discrete-time analog signal having a first throughput rate, said system comprising:
   (a) a quantizer circuit, wherein the discrete-time analog signal is received and converted to a first digital signal having the first throughput rate;
   (b) a digital feedback circuit having a plurality of pipeline stages, wherein the first digital signal is processed at a second throughput rate that is higher than the first throughput rate;
   (c) a feedback digital-to-analog converter, wherein a discrete-time analog feedback signal having the first throughput rate is generated and delayed in time relative to the received discrete-time analog signal; and
   (d) a loop filter, wherein the discrete-time analog feedback signal is provided to the quantizer.

2. The system of claim 1, wherein said first digital signal is a multi-bit digital signal.

3. The system of claim 1, wherein said digital feedback circuit applies digital dither to the first digital signal.

4. The system of claim 3, wherein the first digital signal is an m-bit digital signal and the digital feedback circuit outputs different sets of n-bits from the m-bit first digital signal as a digitally dithered feedback signal, where m is greater than n.

5. The system of claim 3, wherein the first digital signal is an m-bit digital signal and the digital feedback circuit randomly selects different sets of n-bits from the m-bit first digital signal to output as a digitally dithered feedback signal, where m is greater than n.

6. The system of claim 1, wherein said digital feedback circuit includes a shuffler circuit.

7. The system of claim 1, wherein said digital feedback circuit includes a dynamic element mismatch circuit.

8. A system for performing feedback processing, comprising:
   (a) a sampler, wherein a received continuous-time analog signal is sampled at a first throughput rate to generate a first discrete-time analog signal having the first throughput rate;
   (b) a quantizer circuit wherein the first discrete-time analog signal is converted to a first digital signal having the first throughput rate;
   (c) a digital feedback circuit having sequential pipeline stages, wherein the first digital signal is processed at a second throughput rate that is higher than the first throughput rate;
   (d) a feedback digital to analog converter, wherein a continuous-time analog feedback signal having the first throughput rate is generated and delayed in time relative to the received continuous-time analog signal; and
   (e) a loop filter, wherein the continuous-time analog feedback signal is provided to the quantizer circuit.

9. The system of claim 8, wherein the first digital signal is a multi-bit digital signal.

10. The system of claim 8, wherein the digital feedback circuit adds digital dither.

11. The system of claim 10, wherein the first digital signal is an m-bit digital signal and the digital feedback circuit outputs different sets of n-bits from

the m-bit first digital signal as a digitally dithered feedback signal, where m is greater than n.

12. The system of claim 10, wherein the first digital signal is an m-bit digital signal and the digital feedback circuit randomly selects different sets of n-bits from the m-bit first digital signal to output as a digitally dithered feedback signal, where m is greater than n.

13. The system of claim 8, wherein said digital feedback circuit includes a shuffler circuit.

14. The system of claim 8, wherein said digital feedback circuit includes a dynamic element mismatch circuit.

15. A system for performing feedback processing of an analog signal, said system comprising:
    (a) a receiver configured to receive said analog signal at a first throughput rate;
    (b) a pipelined circuit configured to process said analog signal at a second throughput rate, wherein said second throughput rate is faster than said first throughput rate; and
    (c) an output path configured to output said processed signal.

16. The system of claim 15, wherein said pipelined circuit comprises a quantizer.

17. The system of claim 16, wherein said pipelined circuit further comprises digital feedback circuitry.

18. The system of claim 17, wherein said pipelined circuit further comprises feedback digital-to-analog converter circuitry.

19. The system of claim 15, wherein said pipelined circuit comprises digital feedback circuitry.

20. The system of claim 19, wherein said pipelined circuit further comprises feedback digital-to-analog converter circuitry.